For most current data sheet and other product
information, visit www.burr-brown.com

Miniature, 1W, 1500Vrms Isolated
UNREGULATED DC/DC CONVERTERS

FEATURES

● **UP TO 85% EFFICIENCY**
● **THERMAL PROTECTION**
● **DEVICE-TO-DEVICE SYNCHRONIZATION**
● **SHORT-CIRCUIT PROTECTION**
● **EN55022 CLASS B EMC PERFORMANCE**
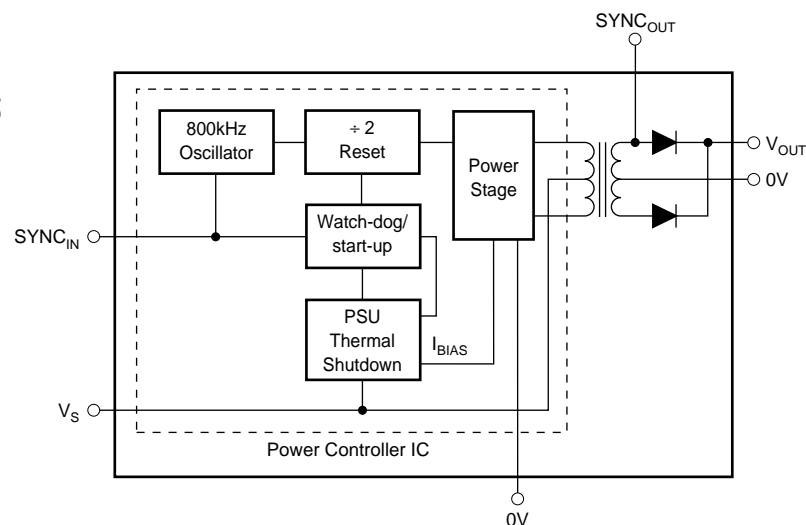● **UL1950 RECOGNIZED COMPONENT**
● **JEDEC PDIP-14 AND GULL-WING PACKAGES**

APPLICATIONS

● **INDUSTRIAL CONTROL AND
  INSTRUMENTATION**
● **POINT-OF-USE POWER CONVERSION**
● **GROUND LOOP ELIMINATION**
● **DATA ACQUISITION**
● **TEST EQUIPMENT**
● **SECONDARY ISOLATION CIRCUITS**

DESCRIPTION

The DCV01 series is a family of 1W, 1500Vrms isolated, unregulated DC/DC converters. Requiring a minimum of external components and including on-chip device protection, the DCV01 series provides extra features such as output disable and synchronization of switching frequencies.

The use of a highly integrated package design results in highly reliable products with a power density of 40W/in^3 (2.4W/cm^3). This combination of features, high isolation, and small size makes the DCV01 suitable for a wide range of applications.

©2000 Burr-Brown Corporation   PDS-1592B   Printed in U.S.A. August, 2000

SPECIFICATIONS

At T_A = +25°C, unless otherwise specified.

PARAMETER	CONDITIONS	DCV01 SERIES MIN	TYP	MAX	UNITS
OUTPUT					
Power	100% Full Load		0.97		W
Ripple	O/P Capacitor = 1µF, 50% Load		20		mVp-p
Voltage vs Temp	Room to Cold		0.046		%/°C
	Room to Hot		0.016		%/°C
INPUT					
Voltage Range on V_S		–10		10	%
ISOLATION					
Voltage	1s Flash Test	1.5			kVrms
	60s Test, UL1950[1]	1.5			kVrms
LINE					
Regulation			1		%/1% of V_S
SWITCHING/SYNCHRONIZATION					
Oscillator Frequency (f_{OSC})	Switching Frequency = f_{OSC}/2		800		kHz
Sync Input Low		0		0.4	V
Sync Input Current	V_{SYNC} = +2V		75		µA
Disable Time			2		µs
Capacitance Loading on $SYNC_{IN}$ Pin	External			3	pF
RELIABILITY					
Demonstrated	T_A = +55°C			75	FITS
THERMAL SHUTDOWN					
IC Temperature at Shutdown			150		°C
Shutdown Current			3		mA
TEMPERATURE RANGE					
Operating		–40		+85	°C

PRODUCT	INPUT VOLTAGE (V) V_S MIN	TYP	MAX	OUTPUT VOLTAGE (V) V_{NOM} 75% LOAD[2] MIN	TYP	MAX	LOAD REGULATION (%) 10% TO 100% LOAD[3] TYP	MAX	NO LOAD CURRENT (mA) I_Q 0% LOAD TYP	EFFICIENCY (%) 100% LOAD TYP	BARRIER CAPACITANCE (pF) C_{ISO} V_{ISO} = 750Vrms TYP	LEAKAGE CURRENT (µA) V_{ISO} = 750Vrms TYP
DCV010505	4.5	5	5.5	4.75	5	5.25	23	31	20	78	3.6	0.9
DCV010505D[4]	4.5	5	5.5	±4.75	±5	±5.25	19	32	23	80	3.8	0.9
DCV010512	4.5	5	5.5	11.4	12	12.6	23	38	30	85	5.1	1.2
DCV010512D	4.5	5	5.5	±11.4	±12	±12.6	19	37	40	82	4.0	1.0
DCV010515	4.5	5	5.5	14.25	15	15.75	30	42	34	84	3.8	0.9
DCV010515D	4.5	5	5.5	±14.25	±15	±15.75	27	41	42	85	4.7	1.1
DCV011512D[4]	13.5	15	16.5	±11.4	±12	±12.6	11	39	19	78	4.2	1.0
DCV011515D[4]	13.5	15	16.5	±14.25	±15	±15.75	12	39	20	79	4.2	1.0
DCV012405[4]	21.6	24	26.4	4.75	5	5.25	13	23	14	77	3.8	0.9
DCV012415D[4]	21.6	24	26.4	±14.25	±15	±15.75	12	35	17	76	5.3	1.3

NOTES: (1) During UL1950 recognition tests only, UL File #E199929. (2) 100% Load Current = 1W/V_{NOM} TYP. (3) Load regulation = (V_{OUT} at 10% – V_{OUT} at 100%)/ V_{OUT} at 75%. (4) Scheduled availability Q4 2000.

ABSOLUTE MAXIMUM RATINGS

Input Voltage:
5V Input Models 7V
15V Input Models 18V
24V Input Models 29V
Storage Temperature .... –60°C to +125°C
Lead Temperature (soldering, 10s) .... 270°C

ORDERING INFORMATION

```
                              DCV01   05   05  (D)  ( )
Basic Model Number: 1W Product ──┘      │    │    │    │
Voltage Input: ──────────────────────────┘    │    │    │
    5V In                                      │    │    │
Voltage Output: ───────────────────────────────┘    │    │
    5V Out                                           │    │
Dual Output: ────────────────────────────────────────┘    │
Package Code:                                              │
    P = PDIP-14 ───────────────────────────────────────────┘
    P-U = PDIP-14 Gull-Wing
```

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
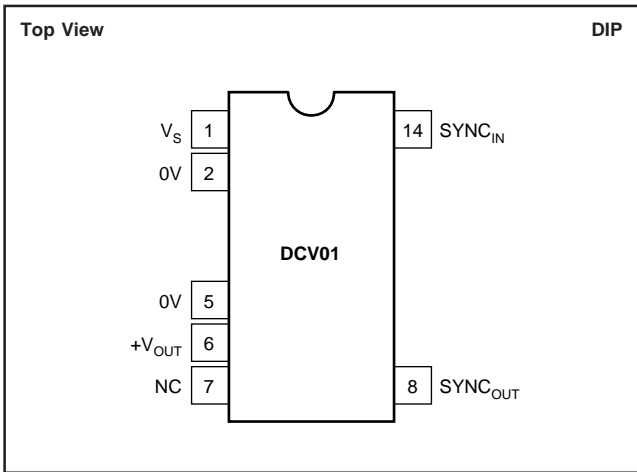
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
Single						
DCV010505P	DIP-14	010-1	–40°C to +85°C	DCV010505P	DCV010505P	Rails
DCV010505P-U	Gull-Wing-14	010-2	–40°C to +85°C	DCV010505P-U	DCV010505P-U/700	Tape and Reel
DCV010512P	DIP-14	010-1	–40°C to +85°C	DCV010512P	DCV010512P	Rails
DCV010512P-U	Gull-Wing-14	010-2	–40°C to +85°C	DCV010512P-U	DCV010512P-U/700	Tape and Reel
DCV010515P	DIP-14	010-1	–40°C to +85°C	DCV010515P	DCV010515P	Rails
DCV010515P-U	Gull-Wing-14	010-2	–40°C to +85°C	DCV010515P-U	DCV010515P-U/700	Tape and Reel
DCV012405P(2)	DIP-14	010-1	–40°C to +85°C	DCV012405P	DCV012405P	Tape and Reel
DCV012405P-U(2)	Gull-Wing-14	010-2	–40°C to +85°C	DCV012405P-U	DCV012405P-U/700	Rails
Dual						
DCV010505DP(2)	DIP-14	010-1	–40°C to +85°C	DCV010505DP	DCV010505DP	Rails
DCV010505DP-U(2)	Gull-Wing-14	010-2	–40°C to +85°C	DCV010505DP-U	DCV010505DP-U/700	Tape and Reel
DCV010512DP	DIP-14	010-1	–40°C to +85°C	DCV010512DP	DCV010512DP	Rails
DCV010512DP-U	Gull-Wing-14	010-2	–40°C to +85°C	DCV010512DP-U	DCV010512DP-U/700	Tape and Reel
DCV010515DP	DIP-14	010-1	–40°C to +85°C	DCV010515DP	DCV010515DP	Rails
DCV010515DP-U	Gull-Wing-14	010-2	–40°C to +85°C	DCV010515DP-U	DCV010515DP-U/700	Tape and Reel
DCV011512DP(2)	DIP-14	010-1	–40°C to +85°C	DCV011512DP	DCV011512DP	Rails
DCV011512DP-U(2)	DIP-14	010-2	–40°C to +85°C	DCV011512DP-U	DCV011512DP-U/700	Tape and Reel
DCV011515DP(2)	Gull-Wing-14	010-1	–40°C to +85°C	DCV011515DP	DCV011515DP	Rails
DCV011515DP-U(2)	DIP-14	010-2	–40°C to +85°C	DCV011515DP-U	DCV011515DP-U/700	Tape and Reel
DCV012415DP(2)	Gull-Wing-14	010-1	–40°C to +85°C	DCV012415DP	DCV012415DP	Rails
DCV012415DP-U(2)	DIP-14	010-2	–40°C to +85°C	DCV012415DP-U	DCV012415DP-U/700	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /700 indicates 700 devices per reel). Ordering 700 pieces of "DCP010505BP-U/700" will get a single 700-piece Tape and Reel. (2) Scheduled availability Q4 2000.

DCV01

BURR - BROWN®
BB

PIN CONFIGURATION (Single-DIP and Gull-Wing)

Top View   **DIP**

V_S | 1 | | 14 | $SYNC_{IN}$
0V | 2 | | |

DCV01

0V | 5 | | |
$+V_{OUT}$ | 6 | | |
NC | 7 | | 8 | $SYNC_{OUT}$

PIN CONFIGURATION (Dual-DIP and Gull-Wing)

Top View   **DIP**

V_S | 1 | | 14 | $SYNC_{IN}$
0V | 2 | | |

DCV01D

0V | 5 | | |
$+V_{OUT}$ | 6 | | |
$-V_{OUT}$ | 7 | | 8 | $SYNC_{OUT}$
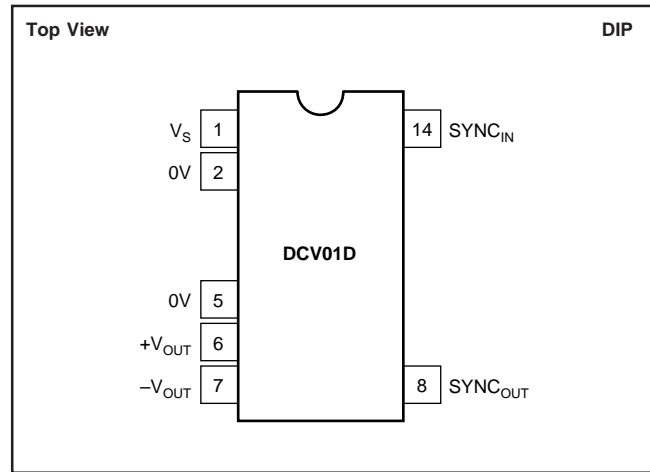
PIN DEFINITION (Single-DIP)

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input
2	0V	Input Side Common
5	0V	Output Side Common
6	$+V_{OUT}$	+Voltage Out
7	NC	Not Connected
8	$SYNC_{OUT}$	Unrectified Transformer Output
14	$SYNC_{IN}$	Synchronization Pin

PIN DEFINITION (Dual-DIP)

PIN #	PIN NAME	DESCRIPTION
1	V_S	Voltage Input
2	0V	Input Side Common
5	0V	Output Side Common
6	$+V_{OUT}$	+Voltage Out
7	$-V_{OUT}$	−Voltage Out
8	$SYNC_{OUT}$	Unrectified Transformer Output
14	$SYNC_{IN}$	Synchronization Pin

TYPICAL PERFORMANCE CURVES

At T_A = +25°C, unless otherwise noted.

DCV010505
OUTPUT RIPPLE vs LOAD (20MHz BW)

DCV010512D V_{OUT} vs LOAD

DCV010512D EFFICIENCY vs LOAD

DCV010515D V_{OUT} vs LOAD

DCV010515D EFFICIENCY vs LOAD

DCV012405 V_{OUT} vs LOAD

BURR - BROWN®
BB
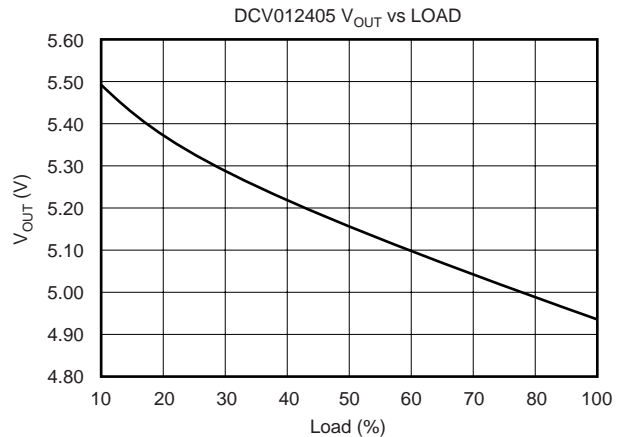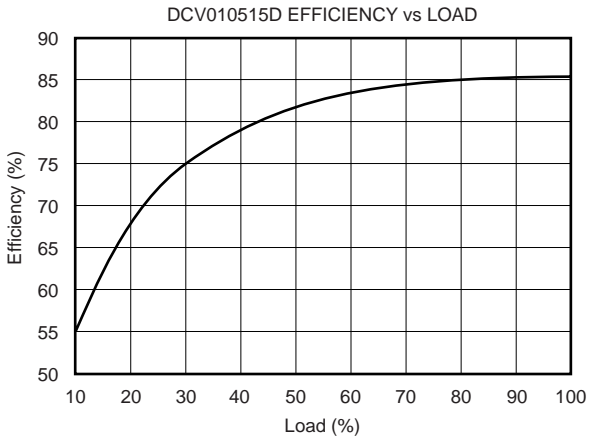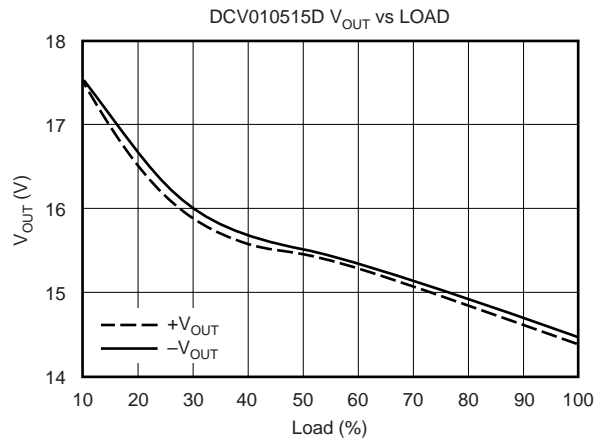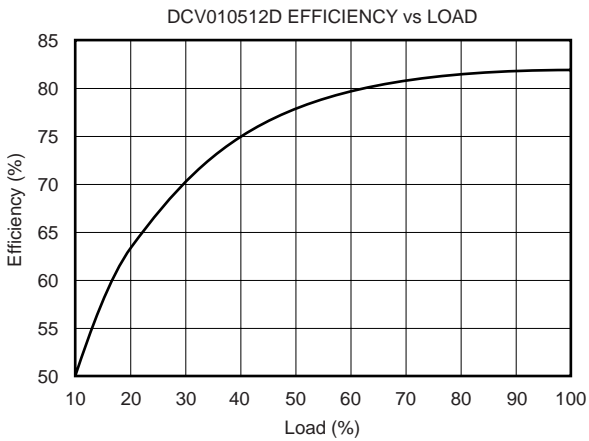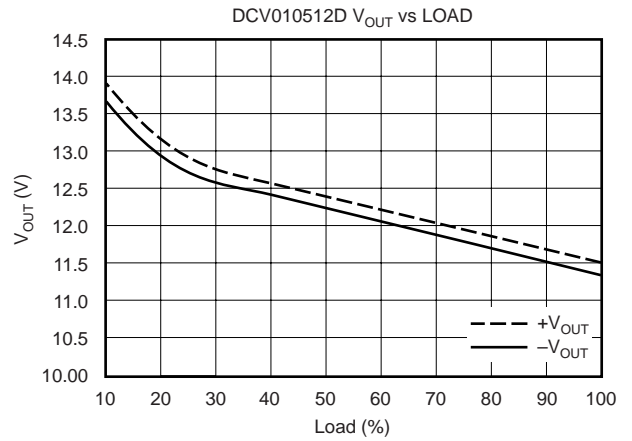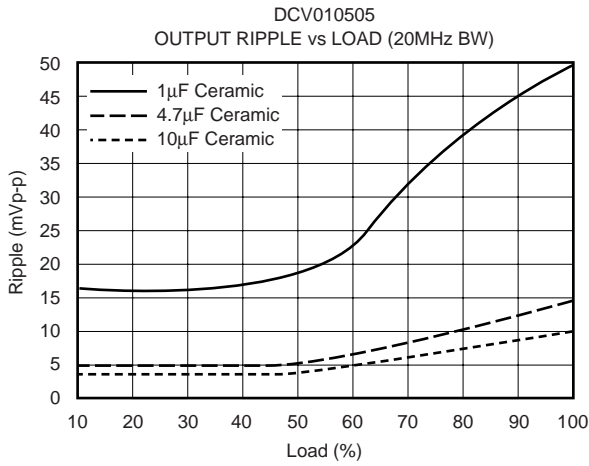
DCV01

TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, unless otherwise noted.

DCV012405 EFFICIENCY vs LOAD

DCV010505
CONDUCTED EMISSIONS (125% Load)

DCV010505
CONDUCTED EMISSIONS (8% Load)
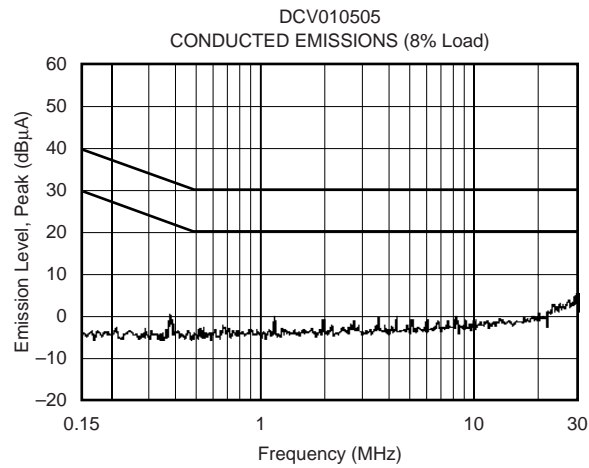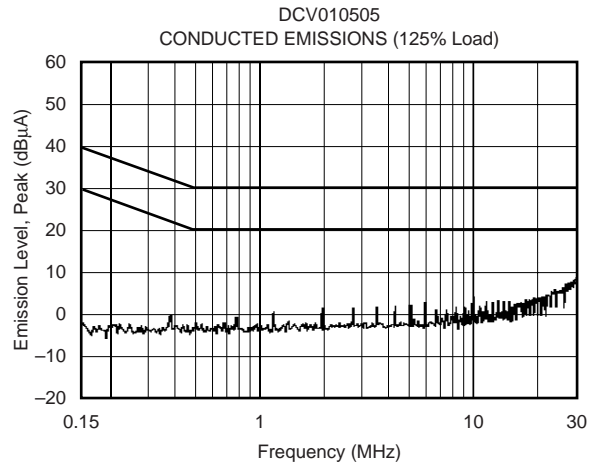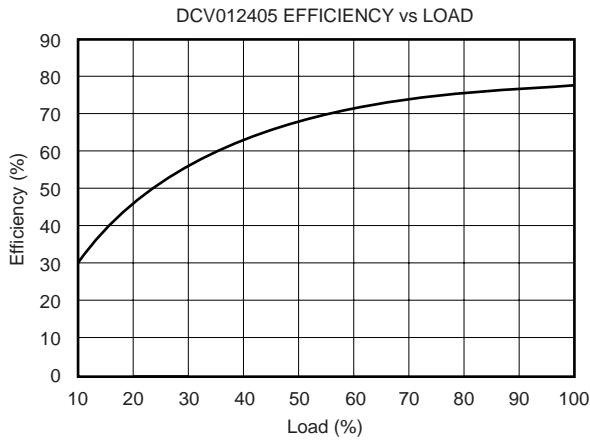
FUNCTIONAL DESCRIPTION

OVERVIEW

The DCV01 offers up to 1W of unregulated output power with a typical efficiency of up to 85%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC. The circuit design utilizes an advanced BiCMOS/DMOS process. Separate primary and secondary transformer windings give good isolation and low barrier capacitance.

POWER STAGE

This uses a push-pull, center-tapped topology switching at 400kHz (divide by 2 from 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The onboard 800kHz oscillator generates the switching frequency via a divide by 2 circuit. The oscillator can be synchronized to other DCV01 circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be stopped by pulling the $SYNC_{IN}$ pin LOW. The output pins will be tri-stated. This will occur in 2μs.

THERMAL SHUTDOWN

The DCV01 is protected by a thermal shutdown circuit. If the on-chip temperature exceeds 150°C, the device will shut down. Once the temperature falls below 150°C, normal operation will resume.

SYNCHRONIZATION

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This is due to the small variations in switching frequencies between the DC/DC converters.

The DCV01 overcomes this by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the $SYNC_{IN}$ pins together, taking care to minimize the capacitance of tracking. Stray capacitance (> 3pF) will have the effect of reducing the switching frequency, or even stopping the oscillator circuit.

If synchronized devices are used, it should be noted that, at start up, all devices will draw maximum current simultaneously. This can cause the input voltage to dip and should it dip below the minimum input voltage (4.5V), the devices may not start up. A 2.2μF capacitor should be connected close to the input pins.

If more than eight devices are to be synchronized, it is recommended that the $SYNC_{IN}$ pins are driven by an external device. Details are contained in a separate applications bulletin (AB-153).

CONSTRUCTION

The DCV01's basic construction is the same as standard ICs. There is no substrate within the molded package. The DCV01 is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. As there is no solder within the package, the DCV01 does not require any special PCB assembly processing. This results in an isolated DC/DC converter with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCV01 can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the $SYNC_{IN}$ pin is pulled low, the DCV01 will be disabled. The disable time depends upon the external loading; the internal disable function is implemented in 2μs. Removal of the pull down will cause the DCV01 to be enabled.

Capacitive loading on the $SYNC_{IN}$ pin should be minimized in order to prevent a reduction in the oscillator frequency.

DECOUPLING

Ripple Reduction

The high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that at least a 1μF capacitor is used on V_{OUT}. Dual outputs should both be decoupled to pin 5. A 2.2μF low ESR capacitor on the input of the 5V in versions, and a 0.47μF low ESR cap on the 24V DCV01 in versions is recommended.
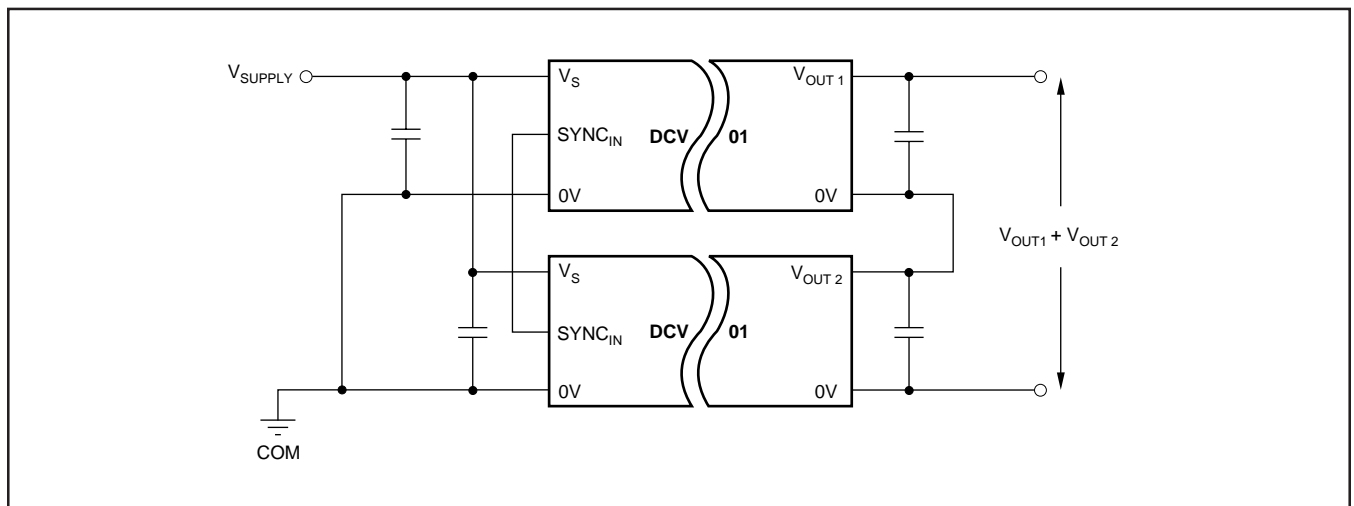

FIGURE 1. Connecting the DCV01 in Series.

DCV01

Connecting the DCV01 in Series

Multiple DCV01 isolated 1W DC/DC converters can be connected in series to provide nonstandard voltage rails. This is possible by utilizing the floating outputs provided by the DCV01's galvanic isolation.

Connect the positive V_{OUT} from one DCV01 to the negative V_{OUT} (0V) of another (see Figure 1). If the $SYNC_{IN}$ pins are tied together, the self-synchronization feature of the DCV01 will prevent beat frequencies on the voltage rails. The $SYNC_{IN}$ feature of the DCV01 allows easy series connection without external filtering, minimizing cost.

The outputs on dual output DCV01 versions can also be connected in series to provide two times the magnitude of V_{OUT} as shown in Figure 2. For example, a dual 15V DCV01 could be connected to provide a 30V rail.

Connecting the DCV01 in Parallel

If the output power from one DCV01 is not sufficient, it is possible to parallel the outputs of multiple DCV01s, as shown in Figure 3. Again, the $SYNC_{IN}$ feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

PCB LAYOUT

Ripple and Noise

Careful consideration should be given to the layout of the PCB in order that the best results can be obtained.

The DCV01 is a switching power supply and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses ground and power planes should be used to track the power to the input of DCV01. If this is not possible then the supplies must be connected in a star formation with the tracks made as wide as possible.

If the $SYNC_{IN}$ pin is being used then the tracking between device $SYNC_{IN}$ pins should be short to avoid stray capacitance. If the $SYNC_{IN}$ pin is not being used it is advisable to place a guard ring, (connected to input ground) around this pin to avoid any noise pick up.

The output should be taken from the device using ground and power planes, this will ensure minimum losses.

A good quality low ESR capacitor placed as close as practicable across the input will reduce reflected ripple and ensure a smooth start up.

A good quality low ESR capacitor placed as close as practicable across the rectifier output terminal and output ground will give the best ripple and noise performance.

THERMAL MANAGEMENT

Due to the high power density of this device it is advisable to provide ground planes on the input and output.
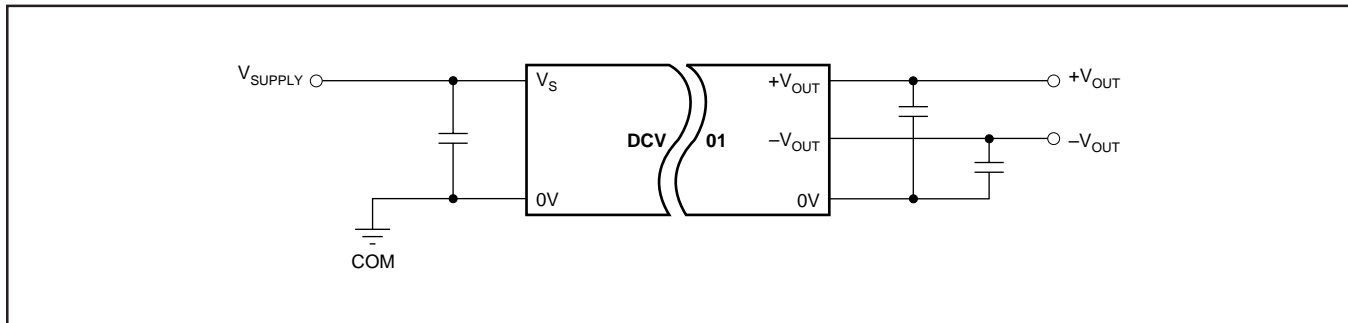

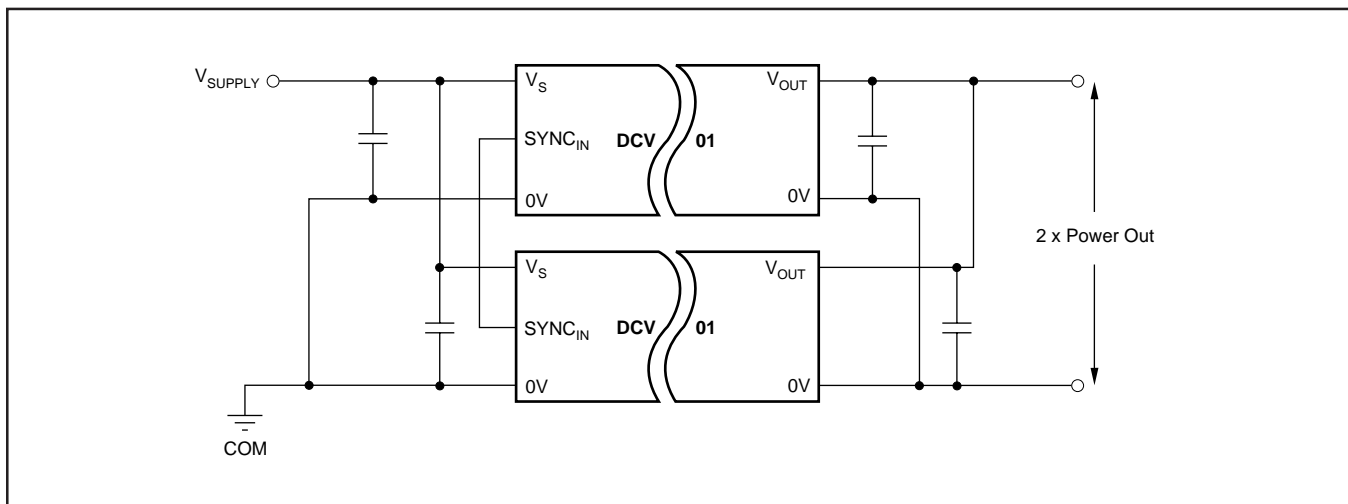FIGURE 2. Connecting Dual Outputs in Series.

FIGURE 3. Connecting Multiple DCV01s in Parallel.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DCV010505DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type
DCV010505DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV010505P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type
DCV010505P-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV010505P-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV010505P-U/700E4	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV010512DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type
DCV010512DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV010512DP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV010512P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type
DCV010512P-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV010515DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type
DCV010515DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV010515P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type
DCV010515P-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV011512DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NiPdAu	N / A for Pkg Type
DCV011512DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NiPdAu	Level-3-260C-168 HR
DCV011512DP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NiPdAu	Level-3-260C-168 HR
DCV011515DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type
DCV011515DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV011515DP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV012405P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type
DCV012405P-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV012405P-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV012415DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	Cu NiPdAu	N / A for Pkg Type

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DCV012415DP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR
DCV012415DP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	Cu NiPdAu	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

NVA (R−PDIP−T7/14) PLASTIC DUAL−IN−LINE

0.775 (19,69) [D]
0.735 (18,67)

14   8

0.280 (7,11)
0.240 (6,10)
[D]

1   7

Index
Area

Base Plane

[H]
0.070 (1,78)
0.045 (1,14)

0.195 (4,95)
0.115 (2,92)

0.210 (5,33) [C]
MAX

−C−

0.015 (0,38)
MIN [C]

0.005 (0,13)
MIN [D]
Full Lead
4 PL

Seating Plane

0.100 (2,54)

0.022 (0,56)
0.014 (0,36)

$\oplus$ 0.010 (0,25) [M] C

0.150 (3,81)
0.115 (2,92)
[C]

0.325 (8,26) [E]
0.300 (7,62)

0.300 (7,63) [E]

0.014 (0,36)
0.008 (0,20)

0.060 (1,52)
0.000 (0,00)
[F]

0.430 (10,92)
MAX [F]

0.800 (20,32)
0.100 (2,54)
0.600 (15,24)

0.038 (0,96)

14   Keep Out Area   8

0.300
(7,63)
0.376
(9,55)

1   7

0.100 (2,54)
3 Places

0.300
(7,63)

ϕ0.036 (0,91) Min. 7 Places
Plated Through Holes

PCB LAYOUT

4202489/B 05/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
[C] Dimensions are measured with the package seated in JEDEC seating plane gauge GS−3.
[D] Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
[E] Dimensions measured with the leads constrained to be perpendicular to Datum C.
[F] Dimensions are measured at the lead tips with the leads unconstrained.
G. Pointed or rounded lead tips are preferred to ease insertion.

[H] Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
J. A visual index feature must be located within the cross−hatched area.
K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
L. Falls within JEDEC MS−001−AA.

TEXAS
INSTRUMENTS
www.ti.com

DUA (R−PDSO−G7/14)   PLASTIC SMALL−OUTLINE

PCB LAYOUT
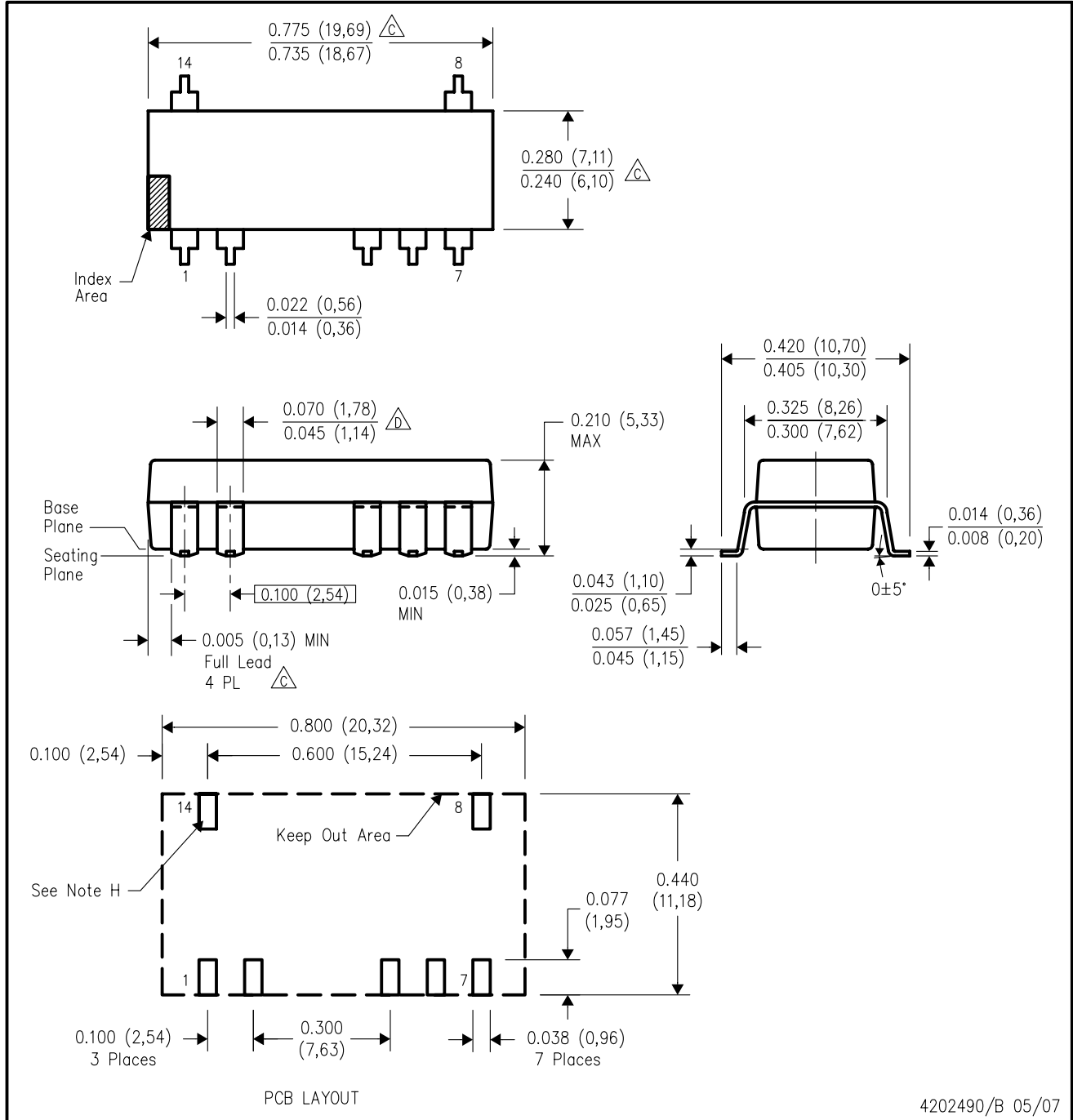
4202490/B 05/07

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Dimensions do not include mold flash or protrusions.
            Mold flash or protrusions shall not exceed 0.010 (0,25).
        D. Lead shoulder maximum dimension does not include
            dambar protrusions. Dambar protrusions shall not
            exceed 0.010 (0,25).
        E. Distance between leads including dambar protrusions
            to be 0.005 (0,13) minimum.
        F. A visual index feature must be located within the
            cross−hatched area.
        G. For automatic insertion, any raised irregularity on the top
            surface (step, mesa, etc.) shall be symmetrical about
            the lateral and longitudinal package centerlines.
        H. Power pin connections should be two or more
            vias per input, ground and output pin.

TEXAS INSTRUMENTS
www.ti.com